Course Description

In “Board Design for Xilinx ZYNQ-7000 SoCs” you learn how to make practical use of XILINX ZYNQ-7000 SoCs. The target audience is not limited to FPGA designers who need to take care of the FPGAs physical interfaces’ integration, but also includes design engineers and PCB layout designers.

The content covers how to resolve design conflicts induced by conflicting requirements between both design teams and offers methods for effective customer project implementations. Power-supply solutions (AC/DC or DC/DC converters, filtering and decoupling) are presented based on given FPGA power requirements (basics and power estimation). Termination required for high clock frequencies and high-speed data rates is covered in detail taking into account different signal levels and termination variants. A special section deals with clock-pulse supply (strategies and implementation) and the connection to high-speed components on the board. Rules of PCB design (PCB tracing, layer stacking) are also explained. Both, Processing System and Programmable Logic board design aspects are discussed in detail.

This course balances lecture modules with practical hands-on labs.

Course Duration

- 2 sessions online (VILT)

Who Should Attend?

- Circuit designers, board layout designers, scientists, engineers and technologists seeking to design PCBs with Xilinx ZYNQ-7000 SoCs

Prerequisites

- FPGA design experience preferred
- Basic knowledge of digital and analog circuit design

Software Tools

- Vivado® Design or System Edition (latest major release)
- Xilinx Power Estimator

Hardware

- Architecture: ZYNQ-7000 SoCs
- Demo board: None
Skills Gained

After completing this comprehensive training, you will have the necessary skills to:

- Describe ZYNQ-7000 SoCs PCB design requirements
- Apply knowledge to design a FPGA power supply
- Select solution options for clock and data interfacing
- Derive and verify design rules for board design
- Describe interface specific requirements and solutions for high-speed interfaces, such as DDR3 or serial transceivers

Course Outline

Session 1

- Course Introduction
- Recovering ZYNQ-7000 SoC Interface Resources and Clocking
- Processing System Interface Requirements
- ZYNQ-7000 SoC Pinning and Packaging
- Lab 1: Pin Planning
- Configuration Requirements and Solutions
- Power Supply – Estimation, Design and Decoupling
- Lab 2: Power Analysis

Session 2

- Signal Interfacing – Requirements and Usage Options
- Termination Options and Usage
- Specific Design Rules (Memory, Transceiver, XADC)
- PCB Technologies and Layer Stackup Definition
- Thermal Aspects
- Lab 3: Thermal Design
- PCB Checklist
- Course Summary

Lab Descriptions

Lab 1: Pin Planning - Use the Vivado software to identify pin placement and implement pin assignments

Lab 2: Power Analysis - Estimate initial power requirements using an Excel spreadsheet, then use the Vivado Power Analyzer to accurately predict board power needs

Lab 3: Thermal Design - Determine maximum junction temperature and calculate acceptable thermal resistance

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