Part II - Designing Memory Interfaces

Course Description
During the complete course (3 parts) you learn how to design DDR4 memory interfaces with Xilinx FPGAs. This part teaches all you need to know about DDR4 memory I/O in Xilinx FPGAs. You should already have knowledge in legacy memory interfacing and you learn Xilinx memory controller design methodology including IP generation, simulation, synthesis and implementation.

This course covers DDR4 memory devices. Labs are available for testing a DDR4 controller on the Kintex®-UltraScale KCU105 board.

You might also want to register for Part III that discusses debugging options and all PCB design aspects.

Course Duration
- 2 sessions online (VILT)

Who Should Attend?
- Designers who already attended to Part I of this course
- Designers that are already familiar with memory designs using previous FPGA generations

Prerequisites
- Participation in Part I of this course or equivalent design experience
- Basic knowledge of FPGA architecture
- Basic knowledge of Xilinx Vivado Design Suite
- FPGA design experience or participation in either „Designing with Verilog“ or „Designing with VHDL“ courses
- Moderate skills in VHDL or in Verilog

Software Tools
- Vivado® Design or System Edition (latest major release)

Hardware
- Architecture: UltraScale FPGAs
- Demo board: Kintex®- UltraScale FPGA KCU105 board

Skills Gained
After completing this comprehensive training, you will have the necessary skills to:
- Recovering FPGAs external memory interface solutions
- Generate memory controller IPs
- Simulate memory interfaces
- Implement memory interfaces
Course Outline

Session 1

- Course Section Introduction
- Recovering UltraScale FPGAs external Memory Interface Solutions
- DDR4 Design Generation
- Lab 1: DDR4 Core Generation
- DDR4 Design Simulation
- Lab 2: DDR4 Design Simulation

Session 2

- DDR4 Design Implementation
- Lab 3: DDR4 Design Implementation
- DDR4 in Embedded Designs
- Lab 4: DDR4 in IP Integrator
- Course Section Summary

Lab Descriptions

Lab 1: DDR4 Core Generation - Create a DDR4 memory controller using the Vivado IP catalog and customize the soft core memory controller for the board

Lab 2: DDR4 Design Simulation - Simulate the memory controller created in Lab 1 using the Vivado simulator

Lab 3: DDR4 Design Implementation - Implement the memory controller created in the previous labs, modify constraints, synthesize, implement, create bitstream, program the FPGA and check the functionality

Lab 4: DDR4 in IP Integrator - Use the block design editor to include the DDR4 IP in a given processor design

Register at https://www.xprosys.net/course-registration/

Additional E-Learning courses available online at https://www.xprosys.net/services/vilt/