Designing an Integrated PCI Express System

PCI Express Gen3 in UltraScale Series FPGAs/SoCs

Course Description
By attending this course students acquire working knowledge of how to implement a Xilinx PCI Express® Gen3 core in custom applications. This course offers students hands-on experience with implementing a Xilinx PCI Express system by using a customer education reference design. With this experience, users can improve their time to market with the PCIe core design. Various Xilinx PCI Express core products will be presented to aid in selecting the proper solution. This course focuses on the AXI streaming client interface.

Course Duration
- 2 sessions online (VILT)

Who Should Attend?
- Hardware designers who want to create applications using Xilinx IP cores for PCI Express Gen3
- Software engineers who want to gain deeper knowledge on how the Xilinx PCI Express solution is working
- System architects who want to leverage key Xilinx advantages related to performance, latency and bandwidth in PCI Express applications

Prerequisites
- Participation in the PCI Express Protocol or equivalent knowledge of the PCIe protocol specification
- Knowledge of VHDL or Verilog
- Some experience with Xilinx implementation tools
- Some experience with a simulation tool, preferably with Vivado® simulator
- Moderate digital design experience

Software Tools
- Vivado Design or System Edition (latest major release)

Hardware
- Architecture: UltraScale Series FPGAs/MPSoCs
- Demo board: Kintex®-UltraScale FPGA KCU105 board

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Skills Gained

After completing this comprehensive training, you will have the necessary skills to:

• Construct a basic PCIe system by:
  • Selecting the appropriate core for your application
  • Specifying requirements of an endpoint application
  • Connecting this endpoint with the core
  • Utilizing FPGA resources to support the core
  • Simulating the design

Course Outline

Session 1

• Course Introduction
• Review PCIe Protocol and Gen3 Improvements
• PCIe Gen3 Core Customization
• **Lab 1: Constructing a PCIe Gen3 Core**
• Simulating a PCIe Gen3 System Design
• Connecting Logic to the Core - AXI Interface
• Packet Formatting Details
• **Lab 2: Downstream Port Model Simulation**

Session 2

• Endpoint Application Considerations
• **Lab 3: Pseudo-Transactional Modeling**
• Application Focus: DMA
• **Lab 4: Design Implementation Packet Formatting Details**
• Root Port Application
• PCIe Configuration
• PCIe Board Design
• Course Summary

Lab Descriptions

**Lab 1: Constructing a PCIe Gen3 Core** - This lab familiarizes you with the necessary flow for generating a Xilinx Integrated PCI Express Endpoint core from the IP catalog. You will select appropriate parameters and create the PCIe core used throughout the labs.

**Lab 2: Downstream Port Model Simulation** - This lab demonstrates timing and behavior of a typical link negotiation using the Vivado simulator. You observe and capture effects of link training and write packets to the endpoint application for later use.

**Lab 3: Pseudo-Transactional Modeling** - This lab illustrates pseudo-transactional modeling which provides various packets to the user design without the need to simulate the PCIe cores themselves.

**Lab 4: Design Implementation** - This lab familiarizes you with all the necessary steps and recommended settings to turn your HDL sources into a bitstream.

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