Part I - Transceiver Design Methodology

Course Description
In this first part you learn how to employ serial transceivers in your UltraScale FPGA designs. You learn how to extend your knowledge to generate, simulate and implement UltraScale FPGAs transceiver designs. Advanced techniques like test and debugging as well as dealing with PCB design challenges are presented in part II. You may also be interested in signing up for this session, too.

This course combines lectures with practical hands-on labs.

Course Duration
• 2 sessions online (VILT)

Who Should Attend?
• Designers familiar with transceiver designs utilizing former FPGA generations

Prerequisites
• Basic knowledge of FPGA architecture
• Basic knowledge of Xilinx Vivado Design Suite
• FPGA design experience or participation in either „Designing with Verilog“ or „Designing with VHDL“ courses
• Moderate skills in VHDL or in Verilog

Software Tools
• Vivado® Design or System Edition (latest major release)
• Vivado simulator
• Optional: Mentor Graphics Questa simulator 10.4 (requires customer license)

Hardware
• Architecture: UltraScale / UltraScale+ FPGAs
• Demo board: Kintex UltraScale FPGA KCU105 board

Skills Gained
After completing this comprehensive training, you will have the necessary skills to:
• Describe UltraScale FPGAs transceivers’ advanced features
• Use UltraScale FPGA’s Transceiver Wizard to instantiate GT primitives in a design
• Simulate and implement transceiver cores
• Use more efficient encoding schemes
• Design and verify your own transceiver core
Course Outline

Session 1
- Course Section Introduction
- UltraScale FPGA's Serial Transceiver Features
- Transceiver Wizard Overview
- **Lab 1**: Transceiver Core Generation
- Simulating a Transceiver Design
- **Lab 2**: Transceiver Simulation

Session 2
- Implementing a Transceiver Design
- **Lab 3**: Transceiver Implementation
- Physical Media Attachments (PMAs)
- Design Methodology
- **Lab 4**: Design Example
- Course Section Summary

Lab Descriptions

**Lab 1**: Transceiver Core Generation - Use UltraScale FPGA's Transceiver Wizard to create instantiation templates

**Lab 2**: Simulation - Use an example design to simulate a transceiver core

**Lab 3**: Implementation - Use an example design to synthesize and implement a transceiver core

**Lab 4**: Design Example - Generate a transceiver design that supports channel bonding over two links, simulate and implement the design and verify its functionality on real hardware

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