Course Description
The second part of this dual part course focuses on practical design steps. This part starts with sRapidIO core configuration. The generated IP core will be simulated and implementation issues are discussed. Finally, a complete sRapidIO link will be designed and tested on real hardware. In doing so, test and debugging options are discussed and practiced. Board design topics are covered as well.

This course combines lectures with practical hands-on labs.

Course Duration
- 2 sessions online (VILT)

Who Should Attend?
- Hardware designers who want to use serial RapidIO interfaces

Prerequisites
- Participation in Part I - Protocol Specification
- Knowledge of VHDL or Verilog
- Moderate digital design experience
- Experience with Xilinx implementation tools

Software Tools
- Vivado Design or System Edition (latest major release)

Hardware
- Architecture: 7 Series FPGAs/MPSoCs
- Demo board: Kintex®-7 FPGA KC705 board

Skills Gained
After completing this comprehensive training, you will have the necessary skills to:
- Use the sRapidIO configuration GUI to instantiate the RapidIO core in a design
- Describe client interface signals
- Simulate sRapidIO designs
- Implement sRapidIO designs
- Debug sRapidIO designs
- Use the sRapidIO IP in embedded designs

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Course Outline

Session 1

- Course Introduction
- Designing with RapidIO
- sRapidIO Core Generation
- Lab 1: Core Generation
- Client Interface - AXI
- sRapidIO Core Simulation
- Lab 2: Core Simulation
- sRapidIO Core Implementation
- Lab 3: Core Implementation

Session 2

- sRapidIO Test and Debugging
- Lab 4: Adding Debug Cores
- Board Design
- Lab 5: Core Debugging
- sRapidIO in Embedded Systems
- Lab 6: sRapidIO IPI Design
- Course Summary

Lab Descriptions

Lab 1: Core Generation - This lab familiarizes you with the necessary flow for generating a Xilinx serial RapidIO core from the IP catalog. You will select appropriate parameters and create the sRapidIO core used throughout the labs.

Lab 2: Core Simulation - This lab demonstrates timing and behavior of a typical link negotiation using the Vivado simulator. You will observe messages and I/O operations.

Lab 3: Core Implementation - This lab familiarizes you with all the necessary steps and recommended settings to turn the HDL source to a bitstream.

Lab 4: Adding Debug Cores - Adding Logic Analyzer Cores into Existing Design - This lab illustrates how to integrate the Vivado logic analyzer into a lab example design.

Lab 5: Core Debugging - This lab illustrates how to use the Vivado logic analyzer to monitor the behavior of the core and a small application for proper operation.

Lab 6: sRapidIO IPI Design - Use the block design editor to include the sRapidIO IP in a given processor design.

Register at https://www.xprosys.net/course-registration/

Additional E-Learning courses available online at https://www.xprosys.net/services/vilt/